



## How to connect a small page NAND Flash memory to STR710

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### Introduction

This document describes the hardware and software necessary to drive an STMicroelectronics Small Page NAND Flash Memory by an STR710. Small Page NAND Flash is a family of non-volatile Flash memories that uses the Single Level Cell (SLC) NAND technology. The devices range from 128Mbits to 1Gbit and operate with either a 1.8V or 3V supply. The size of a Page is 528 Bytes (512 + 16 spare) with a x8 bus width.

The devices covered by this Application Note are:

- NAND128W3A
- NAND256W3A
- NAND512W3A
- NAND01GW3A

Small Page NAND Flash devices are connected using STR710 External Memory Interface (EMI) without glue logic.

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# 1 Signal descriptions

The following tables summarize the signals used in this application note. [Table 1](#) describes all the Small Page NAND Flash signals.

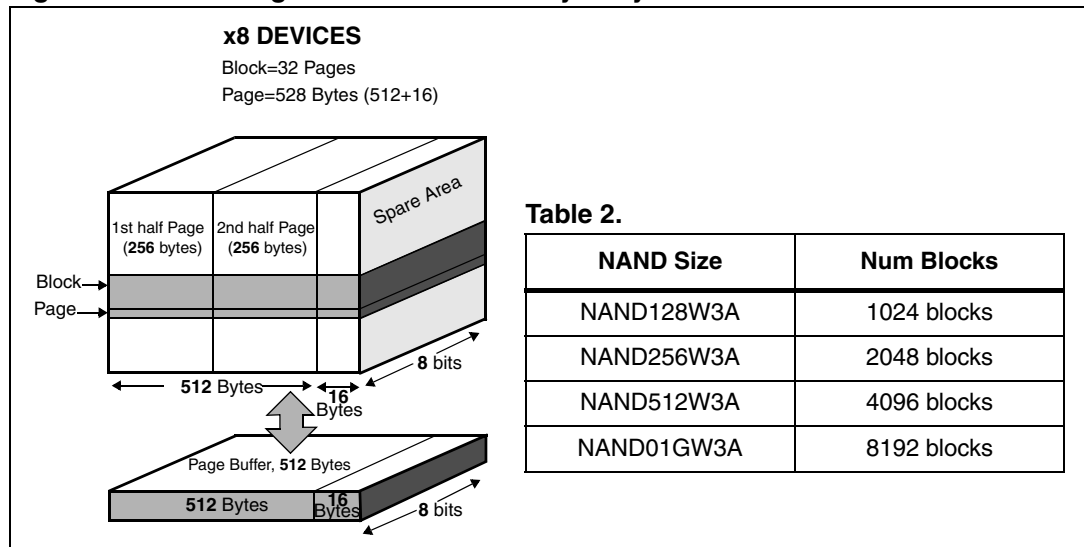
**Table 1. Small Page NAND Flash Signal Descriptions**

Signal	Signal Name	Description
I/O0-I/O7	Data Input/Outputs	Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.
ALE	Address Latch Enable	The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When ALE is high, the inputs are latched on the rising edge of Write Enable.
CLE	Command Latch Enable	The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CLE is high, the inputs are latched on the rising edge of Write Enable.
CE	Chip Enable	The Chip Enable input activates the memory control logic, input buffers, decoders and read circuitry. When Chip Enable is low (VIL) the device is selected. If Chip Enable goes High (VIH) while the device is busy, the device remains selected and does not go into standby mode.
RE	Read Enable	The Read Enable, RE, controls the sequential data output during Read operations. Data is valid tRLQV after the falling edge of RE. The falling edge of RE also increments the internal column address counter by one.
WE	Write Enable	The Write Enable input, WE, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable. During power-up and power-down a recovery time of 10 $\mu$ s (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.
WP	Write Protect	The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, VIL, the device does not accept any program or erase operations. It is recommended to keep the Write Protect pin Low, VIL, during power-up and power-down.
RB	Ready/Busy	The Ready/Busy output, RB, is an open-drain output that can be used to identify if the P/E/R Controller is currently active. When Ready/Busy is Low (VOL) a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High (VOH). The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

## 2 Memory array organization

The memory array is made up of NAND structures where 16 cells are connected in series. The Small Page NAND Flash devices described in this application note have a x8 bus width. The memory array is organized in blocks where each block contains 32 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store error correction codes, software flags or bad block identification. So each pages are split into a main area with two half pages of 256 Bytes each and a spare area of 16 Bytes.

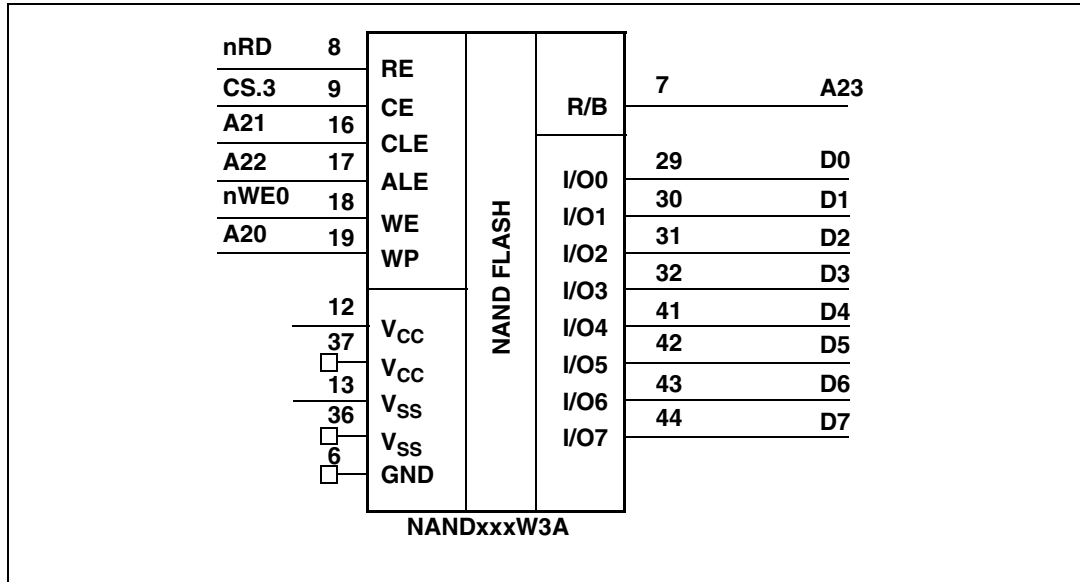
**Figure 1. Small Page NAND Flash memory array blocks**



### 3 Hardware interface

The Small Page NAND Flash NANDxxx3WA is connected with STR710 using an External Memory Interface (EMI) bus, without glue logic.

**Figure 2. NANDxxx3WA signal mapping with STR710**



In this application note, NAND Flash Memory is mapped on EMI bank3, so Memory Chip Enable is connected with CS.3 STR71x signal memory and I/O0..I/O7 are connected with D0..D7 microcontroller EMI bus data signals. Memory control signals are connected with A23..A20 EMI bus address signals. Refer to the table below for further details:

**Table 3. NAND Flash and STR710 EMI Bus signal connections**

NAND Flash signals	STR710 EMI Bus signals
I/O 0..7	D0..D7
RE	nRD
CE	CS.3 (GPIO 2.3)
CLE	A21 (GPIO 2.5)
ALE	A22(GPIO 2.6)
WE	nWE0
WP	A20 (GPIO 2.7)
RB	A23 (GPIO 2.4)

## 4 Firmware

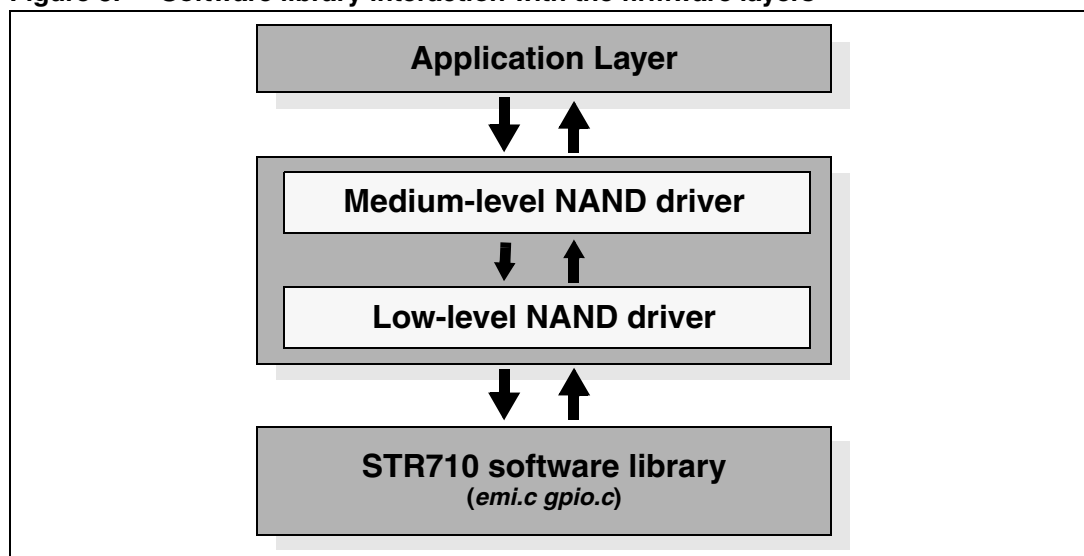
The Software library is organized in two files, *Nand\_flash.h* and *Nand\_flash.c*

In the header file, *nand\_flash.h*, there are device definitions, type definitions and function prototypes. In the file *nand\_flash.c*, all the functions to use the NAND flash device are implemented.

The firmware is developed in two layers, one low-level driver to implement basic NAND Flash functions and a medium-level driver to implement NAND Flash complex functions.

The firmware also includes a module to configure GPIO and EMI from the STR710 standard software library.

**Figure 3. Software library interaction with the firmware layers**



### 4.1 NAND basic functions

There are five standard basic operations controlling the memory:

**Command Input** : `NandCommand (Command Type)`

Command Input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable Is High. All bus write operations to the device are interpreted by the Memory Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Command Registers are summarized in the following table.

**Table 4. Command registers**

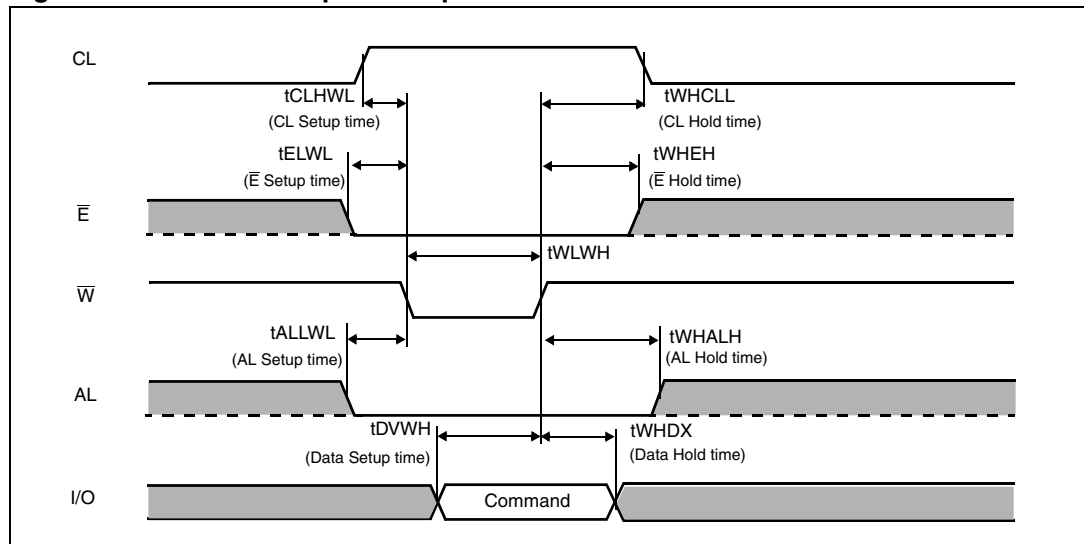
Command	Bus Write Operations <sup>1)</sup>			Command accepted during busy
	1st Cycle	2nd Cycle	3rd Cycle	
Read A	00h			
Read B	01h <sup>2)</sup>			
Read C	50h			
Read Electronic Signature	90h			
Read Status Register	70h			Yes
Page Program	80h	10h		
Copy Back Program	00h	8Ah	10h	
Block Erase	60h	D0h		
Reset	FFh			Yes

Command Types are defined inside the file *nand\_flash.h*

```
#define Nand_AreaA           0x00
#define Nand_AreaB           0x01
#define Nand_AreaC           0x50
#define Nand_ReadStatusReg  0x70
#define Nand_PageProgram     0x80
#define Nand_EndPageProg     0x10
#define Nand_ReadElectSign   0x90
#define Nand_BlockErase      0x60
#define Nand_ConfirmErase    0xD0
#define Nand_Reset           0xFF
#define Nand_CopyBack        0x8A
```

Command Latch Waveforms are :

**Figure 4. Command Input bus operations**



**Address Input :** NandSendAddress (address)

Address Input bus operations are used to input the memory address. Three bus cycles are required to input the addresses for the 128Mb and 256Mb devices and four bus cycles are required to input the addresses for the 512Mb and 1Gb devices (refer to the following Tables, Address Insertion).

**Table 5. Bus cycles required to input addresses**

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O31	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	A16	A15	A14	A13	A12	A11	A10	A9
3rd	A24	A23	A22	A21	A20	A19	A18	A17
4th <sup>4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	A26	A25

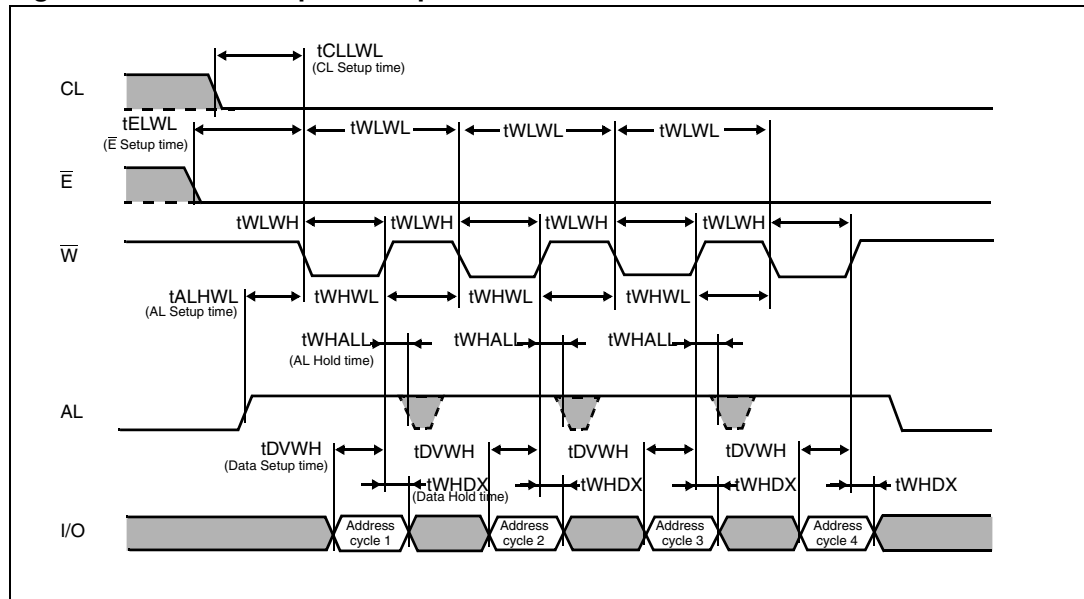
**Table 6. Address definitions**

Address	Definition
A0 - A7	Column Address
A9 - A26	Page Address
A9 - A13	Address in Block
A14 - A26	Block Address
A8	A8 is set Low or High by the 00h or 01h Command, and is Don't Care in x16 devices

A8 is used, by command, to select Area A (1st Half Page) or Area B (2nd Half Page).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

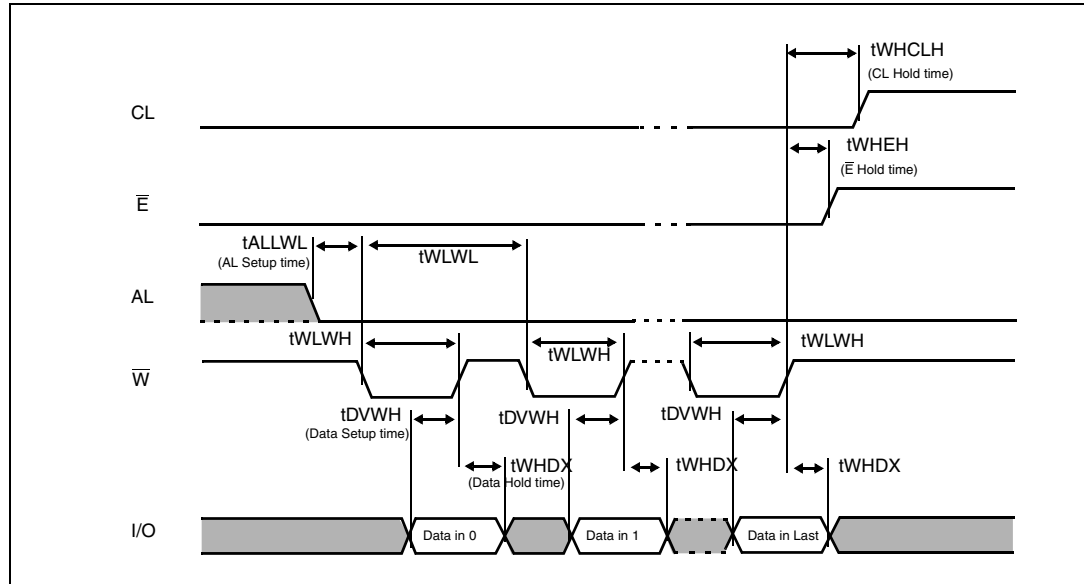
**Figure 5. Address Input bus operations**



**Data Input :** NandDataInput (data)

Data Input bus operations are used to input the data to be programmed. Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

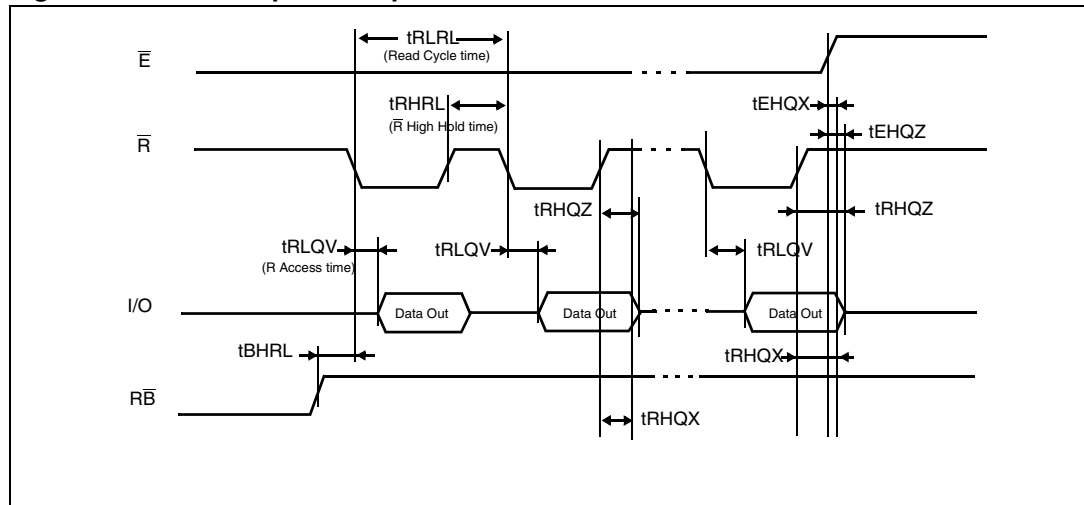
**Figure 6. Data Input bus operations**



**Data Output :** NandDataOutput ( )

Data Output bus operations are used to read the data in the memory array, the Status Register, the Electronic Signature and the Serial Number. Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.

**Figure 7. Data Output bus operations**



**Write Protect :** `Nand_WriteProtect` and `Nand_WriteUnprotect`

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations so that the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

## 4.2 NAND functions

**Flash Initialization :** `NandFlashInit()`

The NAND Flash Memory is set on bank 3 of STR710 EMI with 15 memory wait states.

Pin A23 (GPIO 2.7) of the microcontroller, connected with pin R/B of the NAND, is configured as an input pin and used to monitor the Memory State (Ready or Busy).

A22 (GPIO 2.6), A20 (GPIO 2.4), CS.3 (GPIO 2.3) of the microcontroller, are respectively connected with ALE, WP and CE of the NAND and are configured as 'push-pull output'. The consequence of this is that it can be controlled by software and not automatically by the EMI microcontroller. In the NAND Flash Init State, ALE is not active, CE is not active and the NAND is not in Write Protect Mode.

Read Status Register:

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation. The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register. After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued.

Therefore if a Read Status Register command is issued during a Random Read cycle a new read command must be issued to continue with a PageRead.

**Table 7. Read status register**

Bit	Name	Logic Level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6	Program / Erase / Read Controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR5, SR4, SR3, SR2, SR1	Reserved	Don't Care	
SR0	Generic Error	'1'	Error - operation failed
		'0'	No Error - operation successful

**Write Protection Bit (SR7).** The Write Protection bit can be used to identify if the device is protected or not.

0: the device is protected and program or erase operations are not allowed.

1: the device is not protected and program or erase operations are allowed.

**P/E/R Controller Bit (SR6).** The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive.

0: the P/E/R Controller is active (device is busy).

1: the P/E/R Controller is inactive (device is ready).

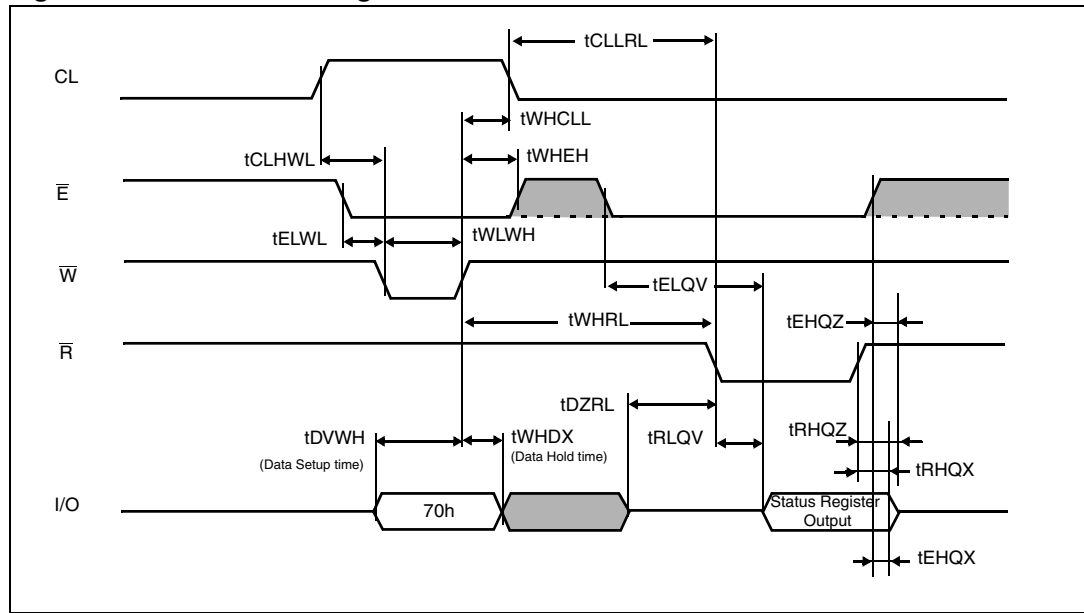
**Error Bit (SR0).** The Error bit is used to identify if any errors have been detected by the P/E/R Controller.

0: no Errors, the operation has completed successfully.

1: Error, a program or erase operation has failed to write the correct data to the memory.

SR5, SR4, SR3, SR2 and SR1 are Reserved.

**Figure 8. Read Status Register**

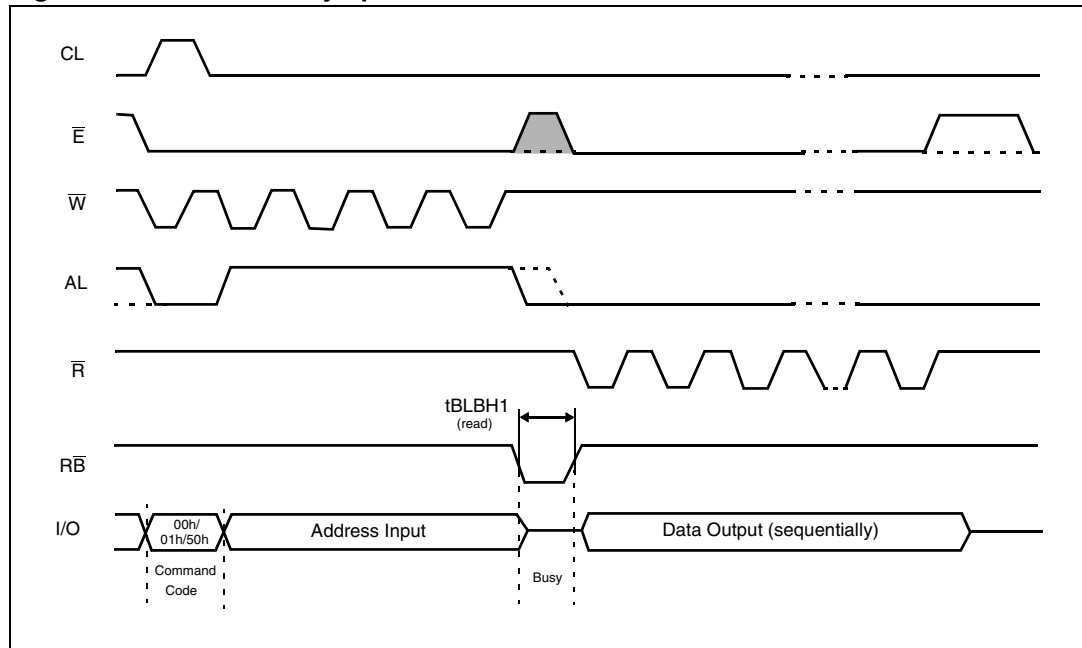


**Read Memory : NandReadData and NandReadNData**

This function permits to read, respectively, 1 or N sequential bytes from NAND Flash memory. Each Read Memory operation consists of six steps:

1. Activate Chip Select (CE)
2. Select Area A or B (1st or 2nd Half Page)
3. Send Address (4 cycles)
4. Monitor R/B pin, until Memory is in Ready State
5. Read one or more Data Byte from the addressed page
6. Disactivate Chip Select (CE)

Figure 9. Read memory operations

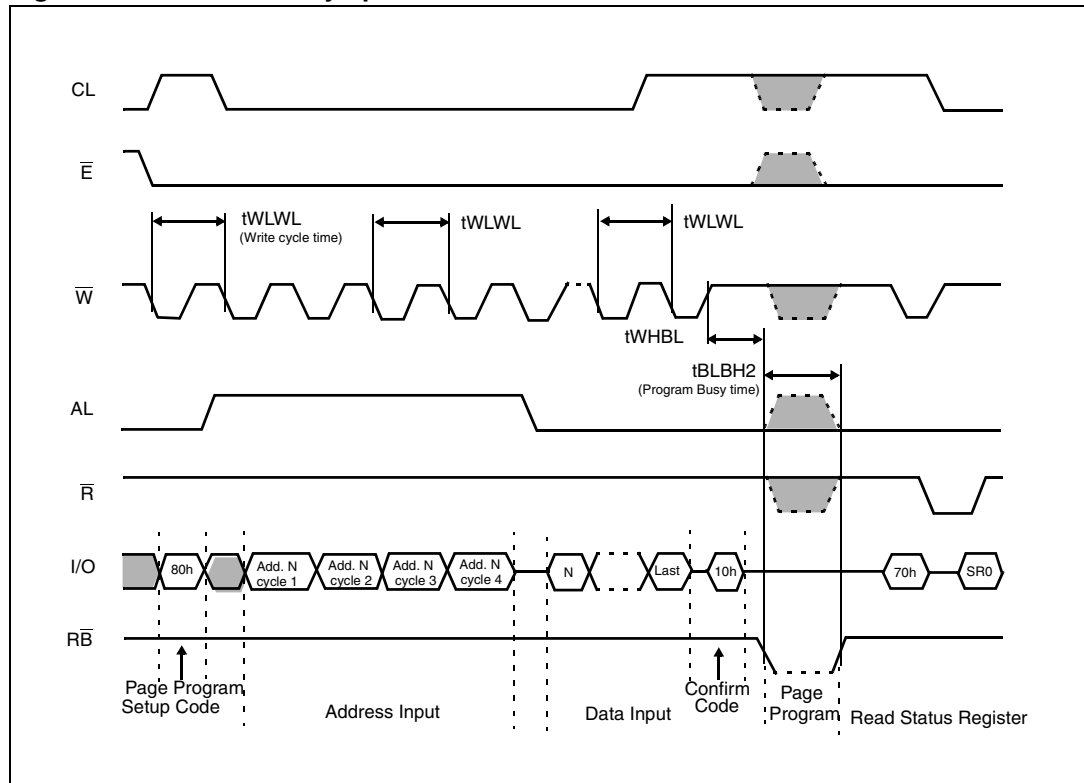


#### Write Memory : NandWriteByte and NandWriteNBytes

The main area (Area A or B) of the memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 528) can be programmed. The maximum number of consecutive partial page program operations allowed in the same page is three. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page. NandWriteByte is used to write only one byte, whereas NandWriteNBytes is used to write N sequential bytes. Each Page Program operation consists of seven steps:

1. Activate CE
2. Send Page Program Command
3. Four bus cycles are then required to input the program address
4. The data is then input (up to 528 Bytes) and loaded into the Page Buffer
5. Send Confirm Page Program Command
6. Monitor R/B pin, until Memory is in Ready State
7. Disactivate Chip Select (CE)

Figure 10. Write memory operations



**Copy Page** : `NandCopyPage(source Address, Dest Address)`

The Copy Back Program operation is used to copy the data stored in one page and reprogram it in another page. The Copy Back Program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the Copy Back Program operation fails an error is signaled in the Status Register. However as the standard external ECC cannot be used with the Copy Back operation bit, any error due to charge loss cannot be detected. For this reason it is recommended to limit the number of Copy Back operations on the same data and or to improve the performance of the ECC.

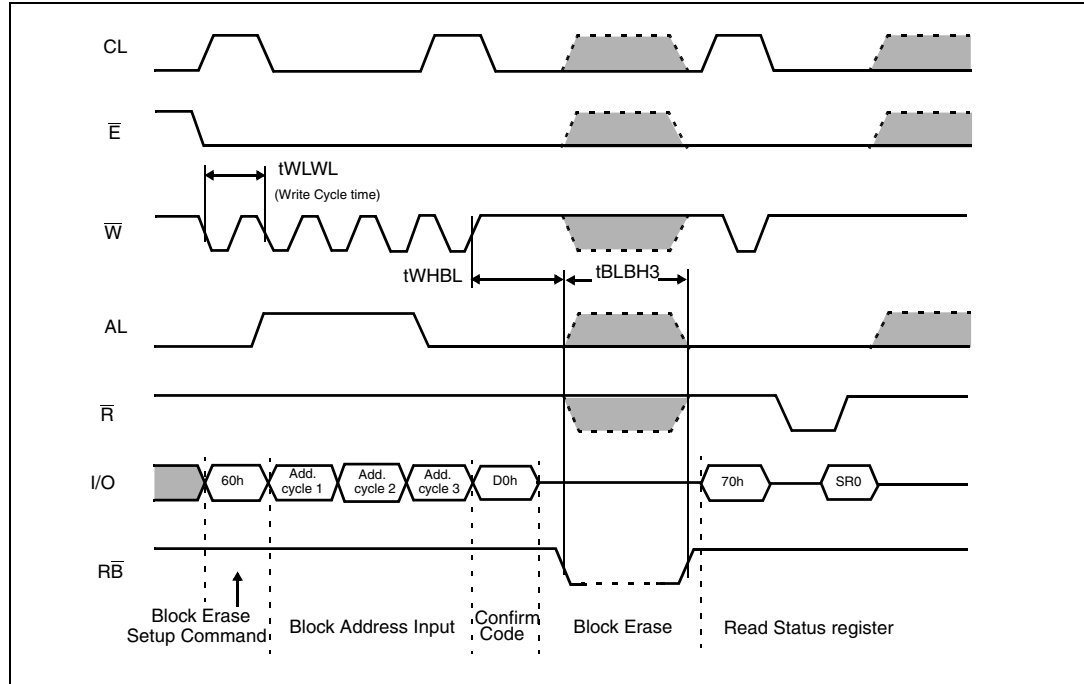
**Block Erase** : `NandBlockErase()`

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to '1'. All previous data in the block is lost.

An erase operation consists of six steps:

1. Activate CE
2. Send Block Erase Command
3. Send Column Address. The first cycle (A0 to A7) is not required as only addresses A14 to A26 (highest address depends on device density) are valid, A9 to A13 are ignored.
4. Send Confirm Block Erase Command
5. Monitor Ready/Busy Memory Pin
6. Disactivate CE

**Figure 11. .Block erase operations**



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
01-Mar-2006	1	Initial release.

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